WEST Search History

DATE: Sunday, May 04, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB; PLUR=YES; OP=ADJ			
L9	L8 and ferroelectric	3	L9
L8	L7 and sense amplifier$1	32	L8
L7	memory and test$ pad$1	148	L7
DB=USPT; PLUR=YES; OP=ADJ			
L6	L5 and ferroelectric	3	L6
L5	L4 and external	142	L5
L4	L3 and sense amplifier$1	160	L4
L3	memory and test$ pad$1	630	L3
DB=JPAB; PLUR=YES; OP=ADJ			
L2	L1 and amplifier$1	3	L2
L1	memory and test$ near2 pad$1	63	L1

END OF SEARCH HISTORY

Generate Collection | Print

Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20020097619 A1

L9: Entry 1 of 3 File: PGPB Jul 25, 2002

PGPUB-DOCUMENT-NUMBER: 20020097619
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020097619 A1

TITLE: Test circuit for an analog measurement of bit line signals of ferroelectric memory cells

PUBLICATION-DATE: July 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Jacob, Michael	Munchen		DE	
Rohr, Thomas	Yokohama City		JP	

US-CL-CURRENT: 365/201; 365/200

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 20020085406 A1

L9: Entry 2 of 3 File: PGPB Jul 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020085406
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020085406 A1

TITLE: Circuit and method for testing a ferroelectric memory device

PUBLICATION-DATE: July 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
McClure, David C.	Carrollton	TX	US	

US-CL-CURRENT: 365/145

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

3. Document ID: US 20020031004 A1

L9: Entry 3 of 3 File: PGPB Mar 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020031004
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020031004 A1

TITLE: Ferroelectric storage device and test method thereof

PUBLICATION-DATE: March 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Miyamoto, Yasuo	Tenri-shi		JP	

US-CL-CURRENT: 365/145

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

Generate Collection Print

Term	Documents
FERROELECTRIC.PGPB.	2581
FERROELECTRICS.PGPB.	377
(8 AND FERROELECTRIC).PGPB.	3
(L8 AND FERROELECTRIC).PGPB.	3

Display Format: CIT Change Format

Previous Page Next Page

a charge on each column line **6** representative of the charge stored in the memory cell **3** connected thereto. Next, signal PRECHARGE is de-asserted, thereby connecting capacitor **44** to the current mirror **43**. With a selected column line **6** being connected to the first current leg **42A** of current mirror **42**, a current flows through first current leg **42A** in proportion to the voltage on column line **6**, which causes a proportional current to flow through second current leg **42B** as well as through first current leg **43A**. A current flows through the second current leg **43B** of current mirror that is proportional to the current in first current leg **43A**, which causes capacitor **44** to collect charges and develop a voltage across capacitor **44**. Following the charging of capacitor **44**, a pad, such as a test pad, may sense the voltage across capacitor **44**. Because the voltage across capacitor **44** is proportional to the voltage that appeared on the selected column line **6**, an accurate indication of the ability of the memory cell **3** connected to the selected column line **6** to charge column line **6** is determined.

[0052] **FIG. 10** is another implementation of current mirror circuitry **21** according to a second embodiment of the present invention. In this case, current mirror circuitry **21** includes a single current mirror **48** having a first current leg **48A** and a second current leg **48B**. A capacitor **49** is connected to the second current leg **48B** via access transistor **50**. A precharge transistor **51** is connected in parallel with the transistor of second current leg **48B**. Control signal PRECHARGE drives the gate terminals of access transistor **50** and precharge transistor **51** so as to precharge capacitor **49** prior to capacitor **49** being connected to current mirror **48**. In operation, connection of a selected column line **6** induces a current in the first current leg **48A** and a proportional current through the second current leg **48B** of current mirror **48**, thereby creating a voltage differential across capacitor **49**. When the charging is complete, a test pad or other pad may be connected across capacitor **49** so as to sense the voltage thereacross. Because the voltage across capacitor **49** is proportional to the currents through current mirror **48** and hence the voltage appearing on the selected column line **6**, a determination of the ability of the memory cell **3** connected thereto may be ascertained.

[0053] Still another embodiment of the present invention is shown in **FIG. 11**. In this case, a current mirror **60** is connected to a single column line **6**, with each column line **6** being connected to a distinct current mirror **60**. Current mirror **60** includes a first current leg **61** connected to a column line **60**, and a second current leg **62** connected to pad **23**. By connecting the common node of current mirror **60** to another pad, such as pad **25**, the transistor in first current leg **61** may be initially biased to the point of conduction, as discussed above with respect to test circuit **20** of **FIG. 4**.

[0054] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. A random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and column lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a column line;

sense amplifier circuitry coupled to the column lines;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to the column lines, for selectively sensing voltage levels appearing on the column lines and providing externally to the random access memory device an electrical signal representative of the sensed voltage levels.

2. The random access memory device of claim **1**, wherein the random access memory device comprises a ferroelectric memory device.

3. The random access memory device of claim **1**, wherein the random access memory device comprises a nonvolatile memory device.

4. The random access memory device of claim **1**, wherein the test circuitry comprises a first current mirror, coupled to the column lines, including a first current leg coupled to the column lines and a second current leg.

5. The random access memory device of claim **4**, wherein the second current leg is coupled to an output pad.

6. The random access memory device of claim **4**, wherein the first current leg is coupled to a plurality of column lines.

7. The random access memory device of claim **6**, wherein the test circuitry further comprises a transmission gate connected between the first current leg of the first current mirror and the column lines coupled thereto.

8. The random access memory device of claim **6**, wherein the test circuitry further comprises a plurality of transmission gates, each transmission gate being connected between the first current leg of the first current mirror and a distinct column line.

9. The random access memory device of claim **4**, wherein a common node between the first and second current legs of the first current mirror is coupled externally to the random access memory device.

10. The random access memory device of claim **4**, wherein the second current leg of the first current mirror is coupled externally to the random access memory device.

11. The random access memory device of claim **11**, wherein the test circuitry further comprises precharge circuitry coupled to the capacitor.

12. The random access memory device of claim **12**, wherein the precharge circuitry comprises a first transistor coupled between the capacitor and a reference voltage source.

13. The random access memory device of claim **4**, wherein:

each of the first and second legs of the first current mirror comprises a transistor connected to a common node; and

the random access memory device further comprises a bias circuit, coupled to the common node, for maintaining the transistors of the first and second current legs of the first current mirror.

14. The random access memory device of claim **13**, wherein:

the bias circuit comprises a test transistor having a first conduction terminal coupled to the common node and

a second conduction terminal coupled externally to the random access memory device, the test transistor having similar operating characteristics to the operating characteristics of the transistors of the first leg of the at least one current mirror.

15. The random access memory device of claim 13, wherein:

the bias circuit comprises a first test transistor having a first conduction terminal coupled to the common node and a second conduction terminal, and a second transistor having a first conduction terminal connected to the second conduction terminal of the first test transistor and a second conduction terminal coupled to a reference voltage line, the first test transistor having similar operating characteristics to the operating characteristics of the transistors of the first leg of the at least one current mirror.

16. The random access memory device of claim 4, wherein:

the first and second current legs of the first current mirror is coupled to a common node; and

the test circuitry further comprises a transistor coupled between the common node and a voltage reference and having a control terminal coupled to a test control signal.

17. The random access memory device of claim 4, wherein the test circuitry further comprises:

a second current mirror having a first current leg coupled to the second current leg of the first current mirror, and a second current leg.

18. The random access memory device of claim 16, wherein the test circuitry further comprises:

a capacitor coupled to the second current leg of the second current mirror, to collect a charge that is proportional to a current level flowing through the second current leg of the second current mirror.

19. The random access memory device of claim 1, wherein:

the test circuitry disables the sense amplifiers during a test operation.

20. The random access memory device of claim 1, wherein the test circuitry converts the sensed voltage levels to current levels and provides the current levels externally to the random access memory device.

21. The random access memory device of claim 1, wherein the test circuitry converts the sensed voltage levels to converted voltage levels and provides the converted voltage levels externally to the random access memory device.

22. The random access memory device of claim 1, wherein the test circuitry comprises a plurality of current mirrors, each current mirror is connected to a distinct column line.

23. A method of testing a semiconductor memory device having an array of memory cells, comprising:

sensing voltage levels appearing in the memory cells; and

providing externally to the semiconductor memory device an electrical signal representative of the sensed voltage levels.

24. The method of claim 23, wherein:

the semiconductor memory device comprises a ferroelectric memory device.

25. The method of claim 23, wherein:

the array of memory cells is arranged into a plurality of rows and columns and includes a plurality of column lines coupled to the columns of memory cells; and

the step of sensing comprises sensing the voltage levels appearing on the column lines.

26. The method of claim 23, further comprising:

converting the sensed voltage levels into current levels that are proportional to the sensed voltage levels.

27. The method of claim 23, further comprising collecting the current on a capacitor.

28. The method of claim 23, further comprising selecting a column line prior to the step of sensing.

29. An integrated circuit, comprising:

a ferroelectric memory device, comprising:

a ferroelectric memory cell; and

test circuitry, coupled to the column lines, for selectively measuring an extent of polarization of the ferroelectric memory cell and providing the measurement externally to the integrated circuit.

30. The integrated circuit of claim 29, wherein:

the test circuitry measures a voltage level maintained in the ferroelectric memory cell and provides externally to the integrated circuit an electrical signal representative of the measured voltage level.

31. The integrated circuit of claim 30, wherein:

the ferroelectric memory cell comprises a ferroelectric capacitor; and

the test circuitry converts a voltage level appearing across the ferroelectric capacitor to a current level and provides the current level externally to the integrated circuit.

32. The integrated circuit of claim 30, wherein the test circuitry comprises a current mirror having a first current leg coupled to the ferroelectric memory cell and a second current leg coupled to a pad on the integrated circuit.

33. The integrated circuit of claim 32, wherein the test circuitry further comprises a plurality of transmission gates connected between the column lines and the first leg of the current mirror.

34. The integrated circuit of claim 32, wherein the test circuitry further comprises a circuit for biasing a common node between the first and second current legs of the current mirror.

* * * * *